What is claimed is:

1. A semiconductor memory device comprising:

a first bit cell array block, in which bit cells thereof are defined by intersections of first bit lines and first word lines, the first bit lines being arranged as pairs of first signal lines and second signal lines, respectively;

a second bit cell array block, in which bit cells thereof are defined by intersections of second bit lines and second word lines, the second bit lines being arranged as pairs of third signal lines and the second signal lines; respectively;

a block division circuit operable to generate and output block division control signals; and

a write bit line divider circuit operable to either open-circuit or connect together the first signal lines and the third signal lines, respectively, according to the block division control signals.

2. The semiconductor memory device of claim 1, further comprising:

a read/write driver operable during a write operation to receive and to process input data and to output as a result thereof write data, and operable during a read operation to sense, to amplify, and then to output bit cell data; and

a scan driver operable during a scan operation to sense, to amplify, and to output the bit cell data.

3. The semiconductor memory device of claim 1, wherein:

the first bit cell array block is operable to receive and to store write data during a write operation, and to read and to output bit cell data during a read or a scan operation; and

the second bit cell array block is operable to receive and to store write data during the write operation, and to read and to output bit cell data during the read or the scan operation.

4. The semiconductor memory device of claim 1, further comprising:

a third bit cell array block, in which bit cells thereof are defined by intersections of third bit lines and third word lines, the third bit lines being

arranged as pairs of fourth signal lines and the second signal lines; respectively; and

a second write bit line divider circuit operable to either open-circuit or connect together the third signal lines and the fourth signal lines, respectively, according to the block division control signals.

5. The semiconductor memory device of claim 4, wherein:

the third bit cell array block is operable to receive and to store write data during a write operation, and to read and to output bit cell data during a read operation or a scan operation.

6. The semiconductor memory device of claim 1, wherein the block division circuit is operable to generate the block division control signals based upon a precharging signal activated during a precharging operation and a write enable signal activated during a write operation.

7. The semiconductor memory device of claim 6, wherein the block division circuit includes:

a NAND circuit operable to perform a NAND operation on the precharging signal and the write enable signal and to output as a result a first one of the block division control signals; and

a logical inverter circuit, which receives and inverts the first one of the block division control signals outputs as a result a second one of the block division control signals.

8. The semiconductor memory device of claim 7, wherein the write bit line divider comprises:

a plurality of NMOSFETs, which receive the first one of the block division control signals through gates thereof, operable to either open-circuit or connect together the first signal lines and the third signal lines, respectively, based upon the first one of the block division control signals; and

a plurality of PMOSFETs, which receive the second one of the block division control signals through gates thereof, operable to either open-circuit or connect

together the first signal lines and the third signal lines, respectively, based upon the second one of the block division control signals.

9. The semiconductor memory device of claim 1, wherein a write operation is performed using double-end bit lines.

10. The semiconductor memory device of claim 1, wherein a read operation is performed using single-end bit lines.

11. The semiconductor memory device of claim 1, wherein a scan operation is performed using single-end bit lines.

12. The semiconductor memory device of claim 1, wherein the bit cells are of a 6T type.

13. A method of driving a semiconductor memory device, the method comprising:

providing a first bit cell array block and a second cell array block;

defining bit cells in the first bit cell array block by intersections of first bit lines and first word lines, the first bit lines being arranged as pairs of first signal lines and second signal lines, respectively;

defining bit cells in the second bit cell array block by intersections of second bit lines and second word lines, the second bit lines being arranged as pairs of third signal lines and the second signal lines; respectively;

generating block division control signals; and

selectively open-circuiting or connecting together the first signal lines and the third signal lines, respectively, according to the block division control signals.

14. The method of claim 13, further comprising:

operating during a write mode by receiving and processing input data and outputting as a result thereof write data;

operating during a read mode by sensing, amplifying, and then outputting bit cell data; and

operating during a scan mode by sensing, amplifying, and then outputting the bit cell data.

15. The method of claim 13, further comprising:

providing a third bit cell array block;

defining bit cells in the third bit cell array block by intersections of third bit lines and third word lines, the third bit lines being arranged as pairs of fourth signal lines and the second signal lines, respectively; and

selectively open-circuiting or connecting together the fourth signal lines and the third signal lines, respectively, according to the block division control signals.

16. The method of claim 13, wherein the generating of the block division control signals includes generating the block division control signals based upon a precharging signal activated during a precharging operation and a write enable signal activated during a write operation.

17. The method of claim 16, further comprising:

performing a NAND operation on the precharging signal and the write enable signal and outputting as a result a first one of the block division control signals; and

inverting the first one of the block division control signals and outputting as a result a second one of the block division control signals.

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